

UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF WASHINGTON

ALTAIR LOGIX LLC,

Plaintiff,

v.

HTC AMERICA INC.,

Defendant.

Case No. 18-cv-1685

COMPLAINT FOR PATENT
INFRINGEMENT

DEMAND FOR JURY TRIAL

Plaintiff Altair Logix LLC files this Complaint for Patent Infringement against HTC America Inc., and would respectfully show the Court as follows:

I. NATURE OF THE LAWSUIT

1. This is an action for patent infringement under the Patent Laws of the United States, Title 35 United States Code (“U.S.C.”) resulting from HTC America Inc. infringing, in an illegal and unauthorized manner and without authorization and/or consent from Altair Logix LLC, United States Patent No. 6,289,434 pursuant to 35 U.S.C. §271, and to recover damages, attorney’s fees, and costs.

II. THE PARTIES

2. Plaintiff Altair Logix LLC (“Altair Logix” or “Plaintiff”) is a Texas limited liability company with its principal place of business at 15922 Eldorado Pkwy, Suite 500 #1513, Frisco, TX 75035.

3. On information and belief, Defendant HTC America Inc. (“Defendant”) is a corporation organized and existing under the laws of Washington, with a place of business

1 at 308 Occidental Ave S, Ste 300, Seattle, WA 98104-2822. Defendant has a registered
2 agent at Cogency Global Inc., 1780 Barnes Blvd SW, Tumwater, WA, 98512-0410.

3
4 **III. JURISDICTION AND VENUE**

5 4. This action arises under the patent laws of the United States, Title 35 of the
6 United States Code. This Court has subject matter jurisdiction of such action under 28
7 U.S.C. §§ 1331 and 1338(a).

8 5. On information and belief, Defendant is subject to this Court's specific and
9 general personal jurisdiction, pursuant to due process and the Washington Long-Arm
10 Statute, due at least to its business in this forum, including at least a portion of the
11 infringements alleged herein. Furthermore, Defendant is subject to this Court's specific
12 and general personal jurisdiction because Defendant is a Washington corporation.

13
14 6. Without limitation, on information and belief, within this State and this
15 District, Defendant has used the patented inventions thereby committing, and continuing to
16 commit, acts of patent infringement alleged herein. In addition, on information and belief,
17 Defendant has derived revenues from its infringing acts occurring within Washington and
18 the Western District of Washington. Further, on information and belief, Defendant is
19 subject to the Court's general jurisdiction, including from regularly doing or soliciting
20 business, engaging in other persistent courses of conduct, and deriving substantial revenue
21 from goods and services provided to persons or entities in Washington and the Western
22 District of Washington. Further, on information and belief, Defendant is subject to the
23 Court's personal jurisdiction at least due to its sale of products and/or services within
24 Washington and the Western District of Washington. Defendant has committed such
25 purposeful acts and/or transactions in Washington and the Western District of Washington
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1 such that it reasonably should know and expect that it could be haled into this Court as a
2 consequence of such activity.

3 7. Venue is proper in this district under 28 U.S.C. § 1400(b). On information
4 and belief, Defendant is incorporated in Washington, and it has a place of business within
5 this District. On information and belief, from and within this District Defendant has
6 committed at least a portion of the infringements at issue in this case.

7 8. For these reasons, personal jurisdiction exists and venue is proper in this
8 Court under 28 U.S.C. § 1400(b).

9
10 **IV. COUNT I**

11 **(PATENT INFRINGEMENT OF UNITED STATES PATENT NO. 6,289,434)**

12 9. Plaintiff incorporates the above paragraphs herein by reference.

13 10. On September 11, 2001, United States Patent No. 6,289,434 (“the ‘434
14 Patent”) was duly and legally issued by the United States Patent and Trademark Office.
15 The application leading to the ‘434 patent was filed on February 27, 1998. (Ex. A at
16 cover).

17 11. The ‘434 Patent is titled “Apparatus and Method of Implementing Systems
18 on Silicon Using Dynamic-Adaptive Run-Time Reconfigurable Circuits for Processing
19 Multiple, Independent Data and Control Streams of Varying Rates.” A true and correct
20 copy of the ‘434 Patent is attached hereto as Exhibit A and incorporated herein by
21 reference.

22 12. Plaintiff is the assignee of all right, title and interest in the ‘434 patent,
23 including all rights to enforce and prosecute actions for infringement and to collect
24 damages for all relevant times against infringers of the ‘434 Patent. Accordingly, Plaintiff
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1 possesses the exclusive right and standing to prosecute the present action for infringement
2 of the '434 Patent by Defendant.

3 13. The invention in the '434 Patent relates to the field of runtime
4 reconfigurable dynamic-adaptive digital circuits which can implement a myriad of digital
5 processing functions related to systems control, digital signal processing, communications,
6 image processing, speech and voice recognition or synthesis, three-dimensional graphics
7 rendering, and video processing. (Ex. A at col. 1:32-38). The object of the invention is to
8 provide a new method and apparatus for implementing systems on silicon or other chip
9 material which will enable the user a means for achieving the performance of fixed-
10 function implementations at a lower cost. (*Id.* at col. 2:64 – col. 3:1).

11 14. The most common method of implementing various functions on an
12 integrated circuit is by specifically designing the function or functions to be performed by
13 placing on silicon an interconnected group of digital circuits in a non-modifiable manner
14 (hard-wired or fixed function implementation). (*Id.* at col. 1:42-47). These circuits are
15 designed to provide the fastest possible operation of the circuit in the least amount of
16 silicon area. (*Id.* at col. 1:47-49). In general, these circuits are made up of an
17 interconnection of various amounts of random-access memory and logic circuits. (*Id.* at
18 col. 1:49-51). Complex systems on silicon are broken up into separate blocks and each
19 block is designed separately to only perform the function that it was intended to do. (*Id.* at
20 col. 1:51-54). Each block has to be individually tested and validated, and then the whole
21 system has to be tested to make sure that the constituent parts work together. (*Id.* at col.
22 1:54-56). This process is becoming increasingly complex as we move into future
23 generations of single-chip system implementations. (*Id.* at col. 1:57-59). Systems
24 implemented in this way generally tend to be the highest performing systems since each
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1 block in the system has been individually tuned to provide the expected level of
2 performance. (*Id.* at col. 1:59-62). This method of implementation may be the smallest
3 (cheapest in terms of silicon area) method when compared to three other distinct ways of
4 implementing such systems. (*Id.* at col. 1:62-65). Each of the other three have their
5 problems and generally do not tend to be the most cost-effective solution. (*Id.* at col. 1:65-
6 67).

8 15. The first way is implemented in software using a microprocessor and
9 associated computing system, which can be used to functionally implement any system.
10 (*Id.* at col. 2:1-2). However, such systems would not be able to deliver real-time
11 performance in a cost-effective manner for the class of applications that was described
12 above. (*Id.* at col. 2:3-5). Their use is best for modeling the subsequent hard-wired/fixed-
13 function system before considerable design effort is put into the system design. (*Id.* at col.
14 2:5-8).

16 16. The second way of implementing such systems is by using an ordinary
17 digital signal processor (DSP). (*Id.* at col. 2:9-10). This class of computing machines is
18 useful for real-time processing of certain speech, audio, video and image processing
19 problems and in certain control functions. (*Id.* at col. 2:10-13). However, they are not
20 cost-effective when it comes to performing certain real time tasks which do not have a
21 high degree of parallelism in them or tasks that require multiple parallel threads of
22 operation such as three-dimensional graphics. (*Id.* at col. 2:13-17).

24 17. The third way of implementing such systems is by using field
25 programmable gate arrays (FPGA). (*Id.* at col. 2:18-19). These devices are made up of a
26 two-dimensional array of fine grained logic and storage elements which can be connected
27 together in the field by downloading a configuration stream which essentially routes
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1 signals between these elements. (*Id.* at col. 2:19-23). This routing of the data is performed
2 by pass-transistor logic. (*Id.* at col. 2:24-25). FPGAs are by far the most flexible of the
3 three methods mentioned. (*Id.* at col. 2:25-26). The problem with trying to implement
4 complex real-time systems with FPGAs is that although there is a greater flexibility for
5 optimizing the silicon usage in such devices, the designer has to trade it off for increase in
6 cost and decrease in performance. (*Id.* at col. 2:26-30). The performance may (in some
7 cases) be increased considerably at a significant cost, but still would not match the
8 performance of hard-wired fixed function devices. (*Id.* at col. 2:30-33).

10 18. These three ways do not reduce the cost or increase the performance over
11 fixed-function systems. (*Id.* at col. 2:35-37). In terms of performance, fixed-function
12 systems still outperform the three ways for the same cost. (*Id.* at col. 2:37-39).

14 19. The three systems can theoretically reduce cost by removing redundancy
15 from the system. (*Id.* at col. 2:40-41). Redundancy is removed by re-using computational
16 blocks and memory. (*Id.* at col. 2:41-42). The only problem is that these systems
17 themselves are increasingly complex, and therefore, their computational density when
18 compared with fixed-function devices is very high. (*Id.* at col. 2:42-45).

20 20. Most systems on silicon are built up of complex blocks of functions that
21 have varying data bandwidth and computational requirements. (*Id.* at col. 2:46-48). As
22 data and control information moves through the system, the processing bandwidth varies
23 enormously. (*Id.* at col. 2:48-50). Regardless of the fact that the bandwidth varies, fixed-
24 function systems have logic blocks that exhibit a “temporal redundancy” that can be
25 exploited to drastically reduce the cost of the system. (*Id.* at col. 2:50-53). This is true,
26 because in fixed function implementations all possible functional requirements of the
27 necessary data processing must be implemented on the silicon regardless of the final
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1 application of the device or the nature of the data to be processed. (*Id.* at col. 2:53-57).

2 Therefore, if a fixed function device must adaptively process data, then it must commit

3 silicon resources to process all possible flavors of the data. (*Id.* at col. 2:58-60).

4 Furthermore, state-variable storage in all fixed function systems are implemented using

5 area inefficient storage elements such as latches and flip-flops. (*Id.* at col. 2:60-63).

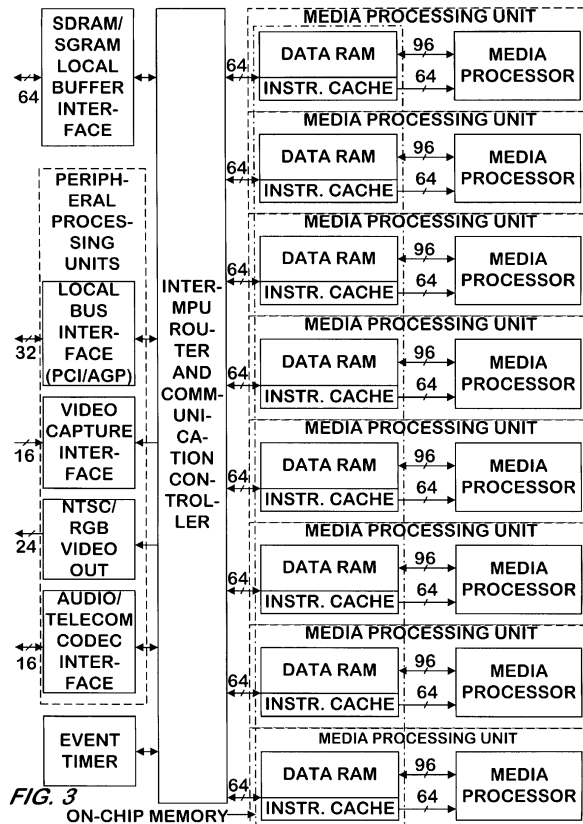
6
7 21. The inventors therefore sought to provide a new apparatus for implementing
8 systems on a chip that will enable the user to achieve performance of fixed-function
9 implementation at a lower cost. (*Id.* at col. 2:64 – col. 3:1). The lower cost is achieved by
10 removing redundancy from the system. (*Id.* at col. 3:1-2). The redundancy is removed by
11 re-using groups of computational and storage elements in different configurations. (*Id.* at
12 col. 3:2-4). The cost is further reduced by employing only static or dynamic ram as a
13 means for holding the state of the system. (*Id.* at col. 3:4-6). This invention provides a
14 way for effectively adapting the configuration of the circuit to varying input data and
15 processing requirements. (*Id.* at col. 3:6-8). All of this reconfiguration can take place
16 dynamically in run-time without any degradation of performance over fixed-function
17 implementations. (*Id.* at col. 3:8-11).

18
19 22. The present invention is therefore an apparatus for adaptively dynamically
20 reconfiguring groups of computations and storage elements in run-time to process multiple
21 separate streams of data and control at varying rates. (*Id.* at col. 3:14-18). The ‘434 patent
22 refers to the aggregate of the dynamically reconfigurable computational and storage
23 elements as a “media processing unit.”

24
25 23. The claimed apparatus has addressable memory for storing data and a
26 plurality of instructions that can be provided through a plurality of inputs/outputs that is
27 couple to the input/output of a plurality of media processing units. (*Id.* at col. 55:21-30).

1 The media processing unit comprises a multiplier, an arithmetic unit, and arithmetic logic
2 unit and a bit manipulation unit. (*Id.* at col. 55:31 – col. 56:20). The ‘434 patent provides
3 examples to explain each of the parts of the media processing unit. (*Id.* at col. 16:27-61
4 (multiplier and adder); *Id.* at col. 16:62 – col. 17:1-9 (arithmetic logic unit); and *Id.* at col.
5 17:10 – col. 17:43 (bit manipulation unit)). Each of the parts has a data input coupled to
6 the media processing unit input/output, an instruction input coupled to the mediate
7 processing unit input/output, and a data output coupled to the mediate processing unit
8 input/output. (*Id.* at col. 55:31 – col. 56:20). Furthermore, the arithmetic logic unit must
9 be capable of operating concurrently with either the multiplier and arithmetic unit. (*Id.* at
10 col. 56:6-12). And the bit manipulation unit must be capable of operating concurrently
11 with the arithmetic logic unit and at least either the multiplier or the arithmetic unit. (*Id.* at
12 col. 56:13-20). Each of the plurality of media processing units must be capable of
13 performing an operating simultaneously with the performance of other operations by other
14 media processing units. (*Id.* at col. 56:21-24). An operation comprises the media
15 processing unit receiving an instruction and data from memory, processing the data
16 responsive to the instruction to produce a result, and providing the result to the media
17 processor input/output. (*Id.* at col. 56:26-33).

21 24. An exemplary block diagram of the claimed systems is shown in Figure 3
22 of the ‘434 patent:



(*Id.* at Fig. 3). Exemplary architecture and coding for the apparatus is disclosed in the '599 patent. (*E.g.*, *Id.* at col. 16:15 – col. 52:20; Figs. 9 – 106).

25. As further demonstrated by the prosecution history of the '434 patent, the claimed invention in the '434 patent was unconventional. Claim 1 of the '434 patent was an originally filed claim that issued without any amendment. There was no rejection in the prosecution history contending that claim 1 was anticipated by any prior art.

26. A key element behind the invention is one of reconfigurability and reusability. (*Id.* at col. 13:26-27). Each apparatus is therefore made up of very high-speed core elements that on a pipelined basis can be configured to form a more complex function. (*Id.* at col. 13:27-30). This leads to a lower gate count, thereby giving a smaller die size and ultimately a lower cost. (*Id.* at col. 13:30-31). Since the apparatuses are virtually identical to each other, writing software becomes very easy. (*Id.* at col. 13:32-

33). The RISC-like nature of each of the media processing units also allows for a consistent hardware platform for simple operating system and driver development. (*Id.* at col. 13:33-36). Any one of the media processing units can take on a supervisory role and act as a central controller if necessary. (*Id.* at col. 13:36-37). This can be very useful in set top applications where a controlling CPU may not be necessary, further reducing system cost. (*Id.* at col. 13:37-40). The claimed apparatus is therefore an unconventional way of implementing processors that can achieve the performance of fixed-function implementations at a lower cost. (*Id.* at col. 2:64 – col. 3:11).

27. **Direct Infringement.** Upon information and belief, Defendant has been directly infringing claims of the ‘434 patent in Washington and the Western District of Washington, and elsewhere in the United States, by making, using, selling, and offering for sale an apparatus for processing data for media processing that satisfies each and every limitation of at least claim 1, including without limitation the HTC One M9 (“Accused Instrumentality”). (*E.g.*, <https://www.htc.com/us/smartphones/htc-one-m9/>).

28. The Accused Instrumentality comprises a processing unit (*e.g.*, Qualcomm Snapdragon 810) which has multiple media processing units (*e.g.*, ARM Quad core Cortex-A53). (*E.g.*, <https://www.htc.com/us/smartphones/htc-one-m9/>; <https://www.techradar.com/reviews/phones/mobile-phones/htc-one-m9-1285623/review>; <https://www.qualcomm.com/products/snapdragon/processors/810>). The Accused Instrumentality comprises an addressable memory (*e.g.*, memory system of the Accused Instrumentality) for storing the data, and a plurality of instructions, and having a plurality of input/outputs, each said input/output for providing and receiving at least one selected from the data and the instructions. As shown below, the Accused Instrumentality comprises a memory system which is coupled to multicore ARM processors through

multiple internal inputs/outputs. The memory system provides instructions and stored data for processing and receives processed data.

Size 144.6 x 69.7 x 9.61 mm	Weight 157g
CPU Speed Qualcomm® Snapdragon™ 810, octa core; 64-bit, 4 x 2.0GHz + 4 x 1.5GHz	Platform Android Android™ with HTC Sense™
Network¹ 2G/2.5G - GSM/GPRS/EDGE: 850/900/1800/1900 MHz 3G UMTS: 850/900/1900/2100 MHz 4G LTE: FDD: Bands 1,3,5,7,8,20,28 TDD: Bands 38, 40, 41	Memory² ROM: 32GB / RAM: 3GB; Extended memory: microSD™ up to 2TB
Connectivity NFC; Bluetooth® 4.1; Wi-Fi®: 802.11 a/b/g/n/ac (2.4 & 5 GHz); DLNA®; HDMI MHL 3.0; CIR; 3.5 mm stereo audio jack; micro-USB 2.0 (5-pin) port	Sound HTC BoomSound™ with Dolby Audio™
Multimedia Audio supported formats: Playback: .aac, .amr, .ogg, .m4a, .mid, .mp3, .wav, .wma, .flac, .ac3, .ec3, .eac3; Recording: .aac Video supported formats: Playback: .3gp, .3g2, .mp4, .wmv, .avi, .mkv; Recording: .mp4	Battery³ Capacity: 2840 mAh; Talk time: Up to 25.4 hours for 2G/ 21.7 hours for 3G; Standby time: Up to 391 hours for 2G/ 402 hours for 3G

(E.g., <https://www.htc.com/us/smartphones/htc-one-m9/>).

1 The internals remain potent: an octa-core Qualcomm 810 chipset, 3GB of RAM,
2 2840 mAh battery on top of a Super LCD3 screen. The latter component hasn't
3 got the cachet of Samsung's Super AMOLED display, but it's still color rich and
4 seems close to the glass, which is important for image quality.



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15 (E.g., [https://www.techradar.com/reviews/phones/mobile-phones/htc-one-m9-](https://www.techradar.com/reviews/phones/mobile-phones/htc-one-m9-1285623/review)
16 [1285623/review](https://www.techradar.com/reviews/phones/mobile-phones/htc-one-m9-1285623/review)).



22 Snapdragon 810 Processor

23
24 As an advanced, connected computing processor with octa-core CPUs, the Qualcomm®
25 Snapdragon™ 810 processor with X10 LTE supports cutting-edge mobile experiences. With
26 download speeds of up to 450 Mbps and the ability to stream 4K Ultra HD video and high-res
27 digital media capabilities, the Snapdragon 810 processor is designed with the connectivity, speed,
28 and power to handle some of today's most demanding tasks and more.

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Fast speeds for greater needs.
X10 LTE supports download speeds of up to 450 Mbps with fully integrated 3x20MHz LTE Advanced carrier aggregation — meaning, with the right network conditions, you can download a full-length HD movie in less than a minute.

Capture the perfect shot.
Dual-Image Signal Processors, autofocus software, and support for a camera of up to 56 megapixels enable you to capture exceptional action shots and low-light stills.

More powerful processing.
With 8-core CPUs and 64-bit computing, Snapdragon 810 enhances your mobile experience by improving processing speed and reducing power consumption.

7 (E.g., <https://www.qualcomm.com/products/snapdragon/processors/810>).

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Bluetooth
Bluetooth Version
• Bluetooth 4.1

Location
Advanced Location Features
• Low Power Geofencing and Tracking
• Sensor-assisted Navigation
• Pedestrian Navigation

CPU
CPU Clock Speed
• Up to 2.0 GHz

CPU Cores
• Octa-core CPU
• 4x ARM Cortex A57
• 4x ARM Cortex A53

CPU Bit Architecture
• 64-bit

16 (E.g., <https://www.qualcomm.com/products/snapdragon/processors/810>).



(E.g., http://media.bestofmicro.com/L/M/479002/original/Snapdragon_810-Overview.jpg).

Overview Documentation	
Architecture	Armv8-A
Multicore	1-4x Symmetrical Multiprocessing (SMP) within a single processor cluster, and multiple coherent SMP processor clusters through AMBA 4 technology
ISA Support	<ul style="list-style-type: none"> • AArch32 for full backward compatibility with Armv7 • AArch64 for 64-bit support and new architectural features • TrustZone security technology • NEON advanced SIMD • DSP & SIMD extensions • VFPv4 floating point • Hardware virtualization support
Debug & Trace	CoreSight DK-A53

(E.

g. <https://developer.arm.com/products/processors/cortex-a/cortex-a53>).

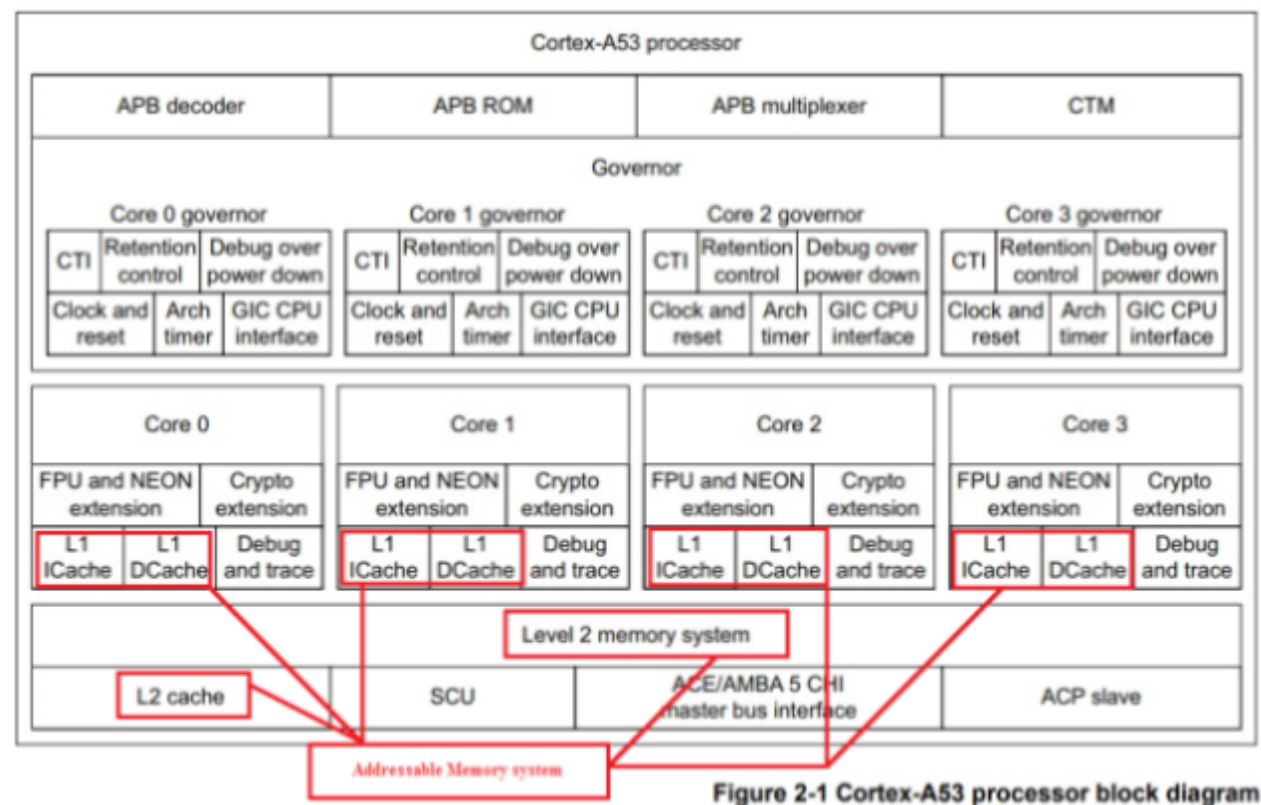


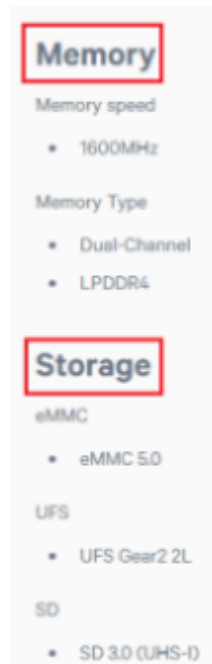
Figure 2-1 Cortex-A53 processor block diagram

(E.g., http://docs-api-peg.northeurope.cloudapp.azure.com/assets/ddi0500/g/DDI0500G_cortex_a53_trm.pdf).

29. The Accused Instrumentality comprises a plurality of media processing units (e.g., ARM cortex-A53 multicore processors), each media processing unit having an input/output coupled to at least one of the addressable memory input/outputs. As shown below, the Accused Instrumentality comprises ARM cortex-A53 multicore processors, each processor comprises a NEON media coprocessor and acts as a media processing unit. The ARM processors are coupled to the memory system. The processors receive instructions and data from the memory system by multiple internal inputs and provides processed data to the memory system by multiple internal outputs.



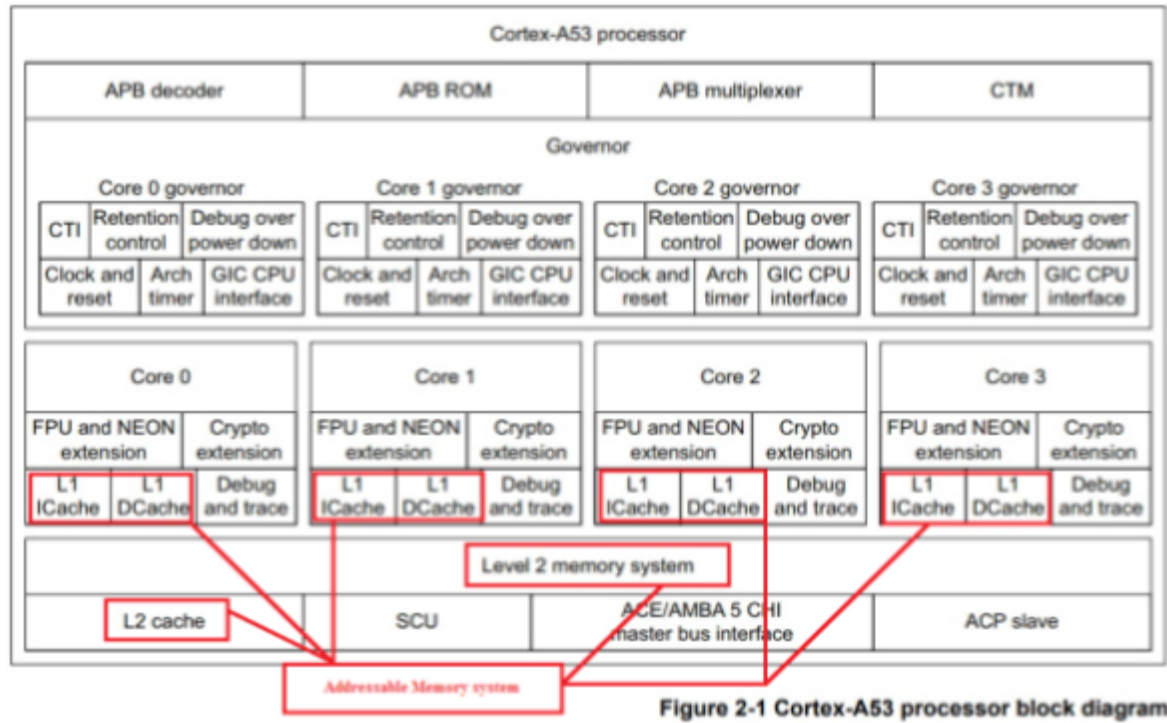
(<https://www.mediatek.com/products/tablets/mt8173>).



(E.g., <https://www.qualcomm.com/products/snapdragon/processors/810>).

Overview Documentation	
Architecture	Armv8-A
Multicore	1-4x Symmetrical Multiprocessing (SMP) within a single processor cluster, and multiple coherent SMP processor clusters through AMBA 4 technology
ISA Support	<ul style="list-style-type: none"> • AArch32 for full backward compatibility with Armv7 • AArch64 for 64-bit support and new architectural features • TrustZone security technology • NEON advanced SIMD • DSP & SIMD extensions • VFPv4 floating point • Hardware virtualization support
Debug & Trace	CoreSight DK-A53

(e.g., <https://developer.arm.com/products/processors/cortex-a/cortex-a53>).



(e.g., http://docs-api-peg.northeurope.cloudapp.azure.com/assets/ddi0500/g/DDI0500G_cortex_a53_trm.pdf).

Advanced SIMD and floating-point Extension

The optional Advanced SIMD and floating-point Extension implements:

- ARM NEON technology, a media, and signal processing architecture that adds instructions that are targeted at audio, video, 3-D graphics, image, and speech processing. Advanced SIMD instructions are available in AArch64 and AArch32 states.

(e.g., http://docs-api-peg.northeurope.cloudapp.azure.com/assets/ddi0500/g/DDI0500G_cortex_a53_trm.pdf).

L2 memory system

The Cortex-A53 L2 memory system contains the L2 cache pipeline and all logic required to maintain memory coherence between the cores of the cluster. It has the following features:

- An SCU that connects the cores to the external memory system through the master memory interface. The SCU maintains data cache coherency between the cores and arbitrates L2 requests from the cores.

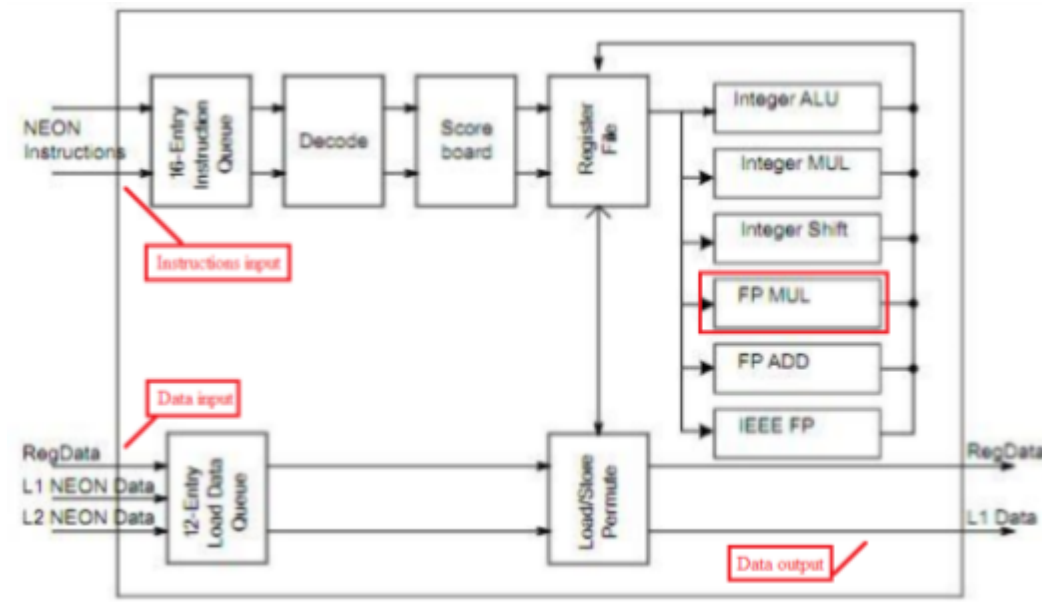
When the Cortex-A53 processor is implemented with a single core, it still includes the *Snoop Control Unit (SCU)*. See *Implementation options on page 1-7* for more information.

(E.g., http://docs-api-peg.northeurope.cloudapp.azure.com/assets/ddi0500/g/DDI0500G_cortex_a53_trm.pdf).

30. The Accused Instrumentality comprises media processors with each processor comprising a multiplier (e.g., an Integer MUL or FP MUL) having a data input coupled to the media processing unit input/output, an instruction input coupled to the media processing unit input/output, and a data output coupled to the media processing unit input/output. As shown below, the Accused Instrumentality comprises multiple ARM cortex-A53 multicore processor, each processor comprises a NEON media coprocessor and acts as a media processing unit. NEON media coprocessor comprises a multiplier which is coupled to the inputs/outputs of the processor. Upon information and belief, the multiplier comprises a data input, an instruction input, and a data output coupled to the input/output of the processor.

Overview	Documentation
Architecture	Armv8-A
Multicore	1-4x Symmetrical Multiprocessing (SMP) within a single processor cluster, and multiple coherent SMP processor clusters through AMBA 4 technology
ISA Support	<ul style="list-style-type: none"> • AArch32 for full backward compatibility with Armv7 • AArch64 for 64-bit support and new architectural features • TrustZone security technology • NEON advanced SIMD • DSP & SIMD extensions • VFPv4 floating point • Hardware virtualization support
Debug & Trace	CoreSight DK-A53

(E.g., <https://developer.arm.com/products/processors/cortex-a/cortex-a53>).



(E.g., <http://www.add.ece.ufl.edu/4924/docs/arm/ARM%20NEON%20Development.pdf>).

31. The Accused Instrumentality comprises media processors with each processor comprising an arithmetic unit (*e.g.*, an FP ADD) having a data input coupled to the media processing unit input/output, an instruction input coupled to the media processing unit input/output, and a data output coupled to the media processing unit input/output. As shown below, the Accused Instrumentality comprises multiple ARM cortex-A53 multicore processor, each processor comprises a NEON media coprocessor and acts as a media processing unit. NEON media coprocessor comprises an arithmetic unit which is coupled to the inputs/outputs of the processor. Upon information and belief, the arithmetic unit comprises a data input, an instruction input, and a data output coupled to the input/output of the processor.

Overview	Documentation
Architecture	Armv8-A
Multicore	1-4x Symmetrical Multiprocessing (SMP) within a single processor cluster, and multiple coherent SMP processor clusters through AMBA 4 technology
ISA Support	<ul style="list-style-type: none"> • AArch32 for full backward compatibility with Armv7 • AArch64 for 64-bit support and new architectural features • <u>TrustZone</u> security technology • <u>NEON advanced SIMD</u> • <u>DSP & SIMD extensions</u> • VFPv4 floating point • Hardware virtualization support
Debug & Trace	<u>CoreSight</u> DK-A53

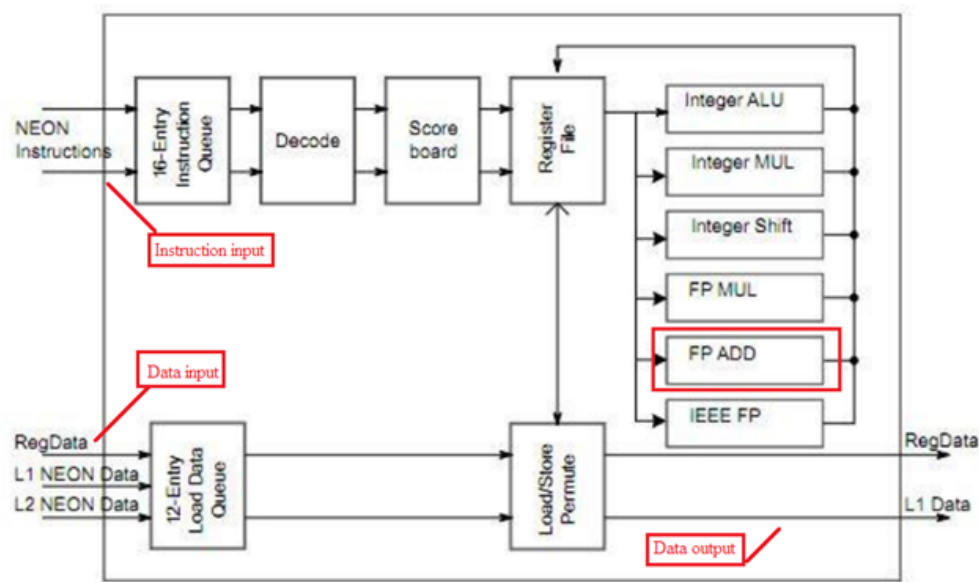
(E.g., <https://developer.arm.com/products/processors/cortex-a/cortex-a53>).

Advanced SIMD and floating-point Extension

The optional Advanced SIMD and floating-point Extension implements:

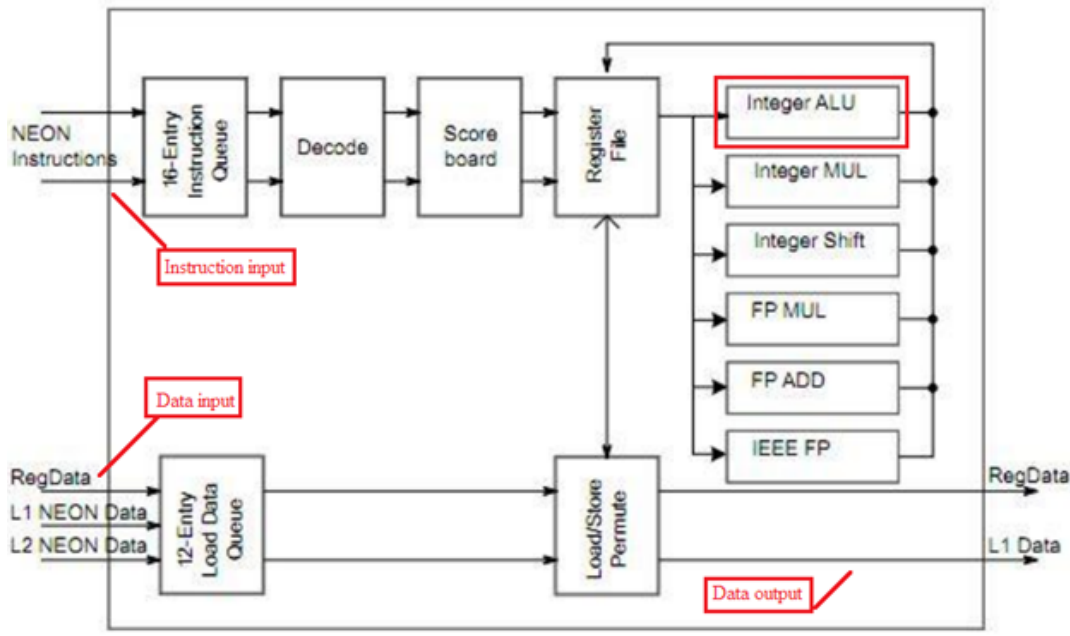
- ARM NEON technology, a media, and signal processing architecture that adds instructions that are targeted at audio, video, 3-D graphics, image, and speech processing. Advanced SIMD instructions are available in AArch64 and AArch32 states.

(E.g., http://docs-api-peg.northeurope.cloudapp.azure.com/assets/ddi0500/g/DDI0500G_cortex_a53_trm.pdf).



1 (E.g., <http://www.add.ece.ufl.edu/4924/docs/arm/ARM%20NEON%20Development.pdf>).

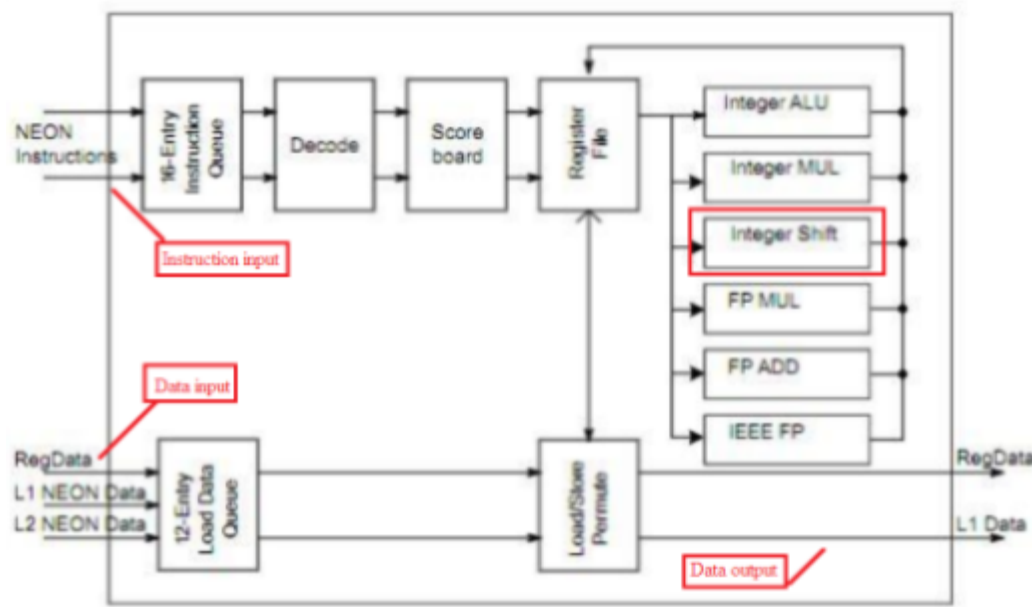
2 32. The Accused Instrumentality comprises media processors with each
3 processor comprising an arithmetic logic unit (e.g., an ALU) having a data input coupled
4 to the media processing unit input/output, an instruction input coupled to the media
5 processing unit input/output, and a data output coupled to the media processing unit
6 input/output, capable of operating concurrently with at least one selected from the
7 multiplier (e.g., an Integer MUL or FP MUL) and arithmetic unit (e.g., a FP ADD). As
8 shown below, the Accused Instrumentality comprises multiple ARM cortex-A53 multicore
9 processor, each processor comprises a NEON media coprocessor and acts as a media
10 processing unit. NEON media coprocessor comprises an arithmetic logical unit which is
11 coupled to the inputs/outputs of the processor. Upon information and belief, the arithmetic
12 logical unit comprises a data input, an instruction input, and a data output coupled to the
13 input/output of the processor. Upon information and belief, the arithmetic logical unit (e.g.,
14 the Integer ALU) is capable of operating concurrently with at least one selected from the
15 multiplier (e.g., the Integer MUL or FP MUL) and arithmetic unit (e.g., the FP ADD).
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(E.g., <http://www.add.ece.ufl.edu/4924/docs/arm/ARM%20NEON%20Development.pdf>).

33. The Accused Instrumentality comprises media processors with each processor comprising a bit manipulation unit (e.g., an Integer Shift unit) having a data input coupled to the media processing unit input/output, an instruction input coupled to the media processing unit input/output, and a data output coupled to the media processing unit input/output, capable of operating concurrently with the arithmetic logic unit (e.g., an Integer ALU) and at least one selected from the multiplier (e.g., an Integer MUL or FP MUL) and arithmetic unit (e.g., a FP ADD). As shown below, the Accused Instrumentality comprises multiple ARM cortex-A53 multicore processors, each processor comprising a NEON media coprocessor that acts as a media processing unit. The NEON media coprocessor comprises an integer shift unit (i.e., bit manipulation unit) which is coupled to the inputs/outputs of the processor. Upon information and belief, the integer shift unit (i.e., bit manipulation unit) comprises a data input, an instruction input, and a data output coupled to the input/output of the processor. Upon information and belief, the

integer shift unit (*i.e.*, bit manipulation unit) is capable of operating concurrently with the arithmetic logic unit (*e.g.*, the Integer ALU) and at least one selected from the multiplier (*e.g.*, the Integer MUL or FP MUL) and arithmetic unit (*e.g.*, the FP ADD).



(*E.g.*, <http://www.add.ece.ufl.edu/4924/docs/arm/ARM%20NEON%20Development.pdf>).

34. The Accused Instrumentality comprises a plurality of media processors (*e.g.*, ARM cortex-A53 multicore processors) for performing at least one operation, simultaneously with the performance of other operations by other media processing units (*e.g.*, other ARM cortex-A53 multicore processors on the same chip).



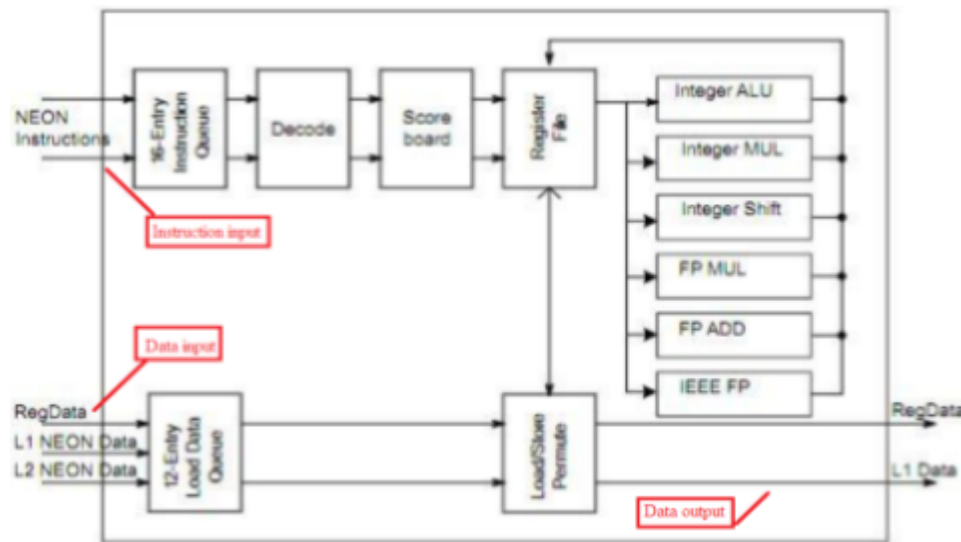
(E.g., http://media.bestofmicro.com/L/M/479002/original/Snapdragon_810-Overview.jpg).



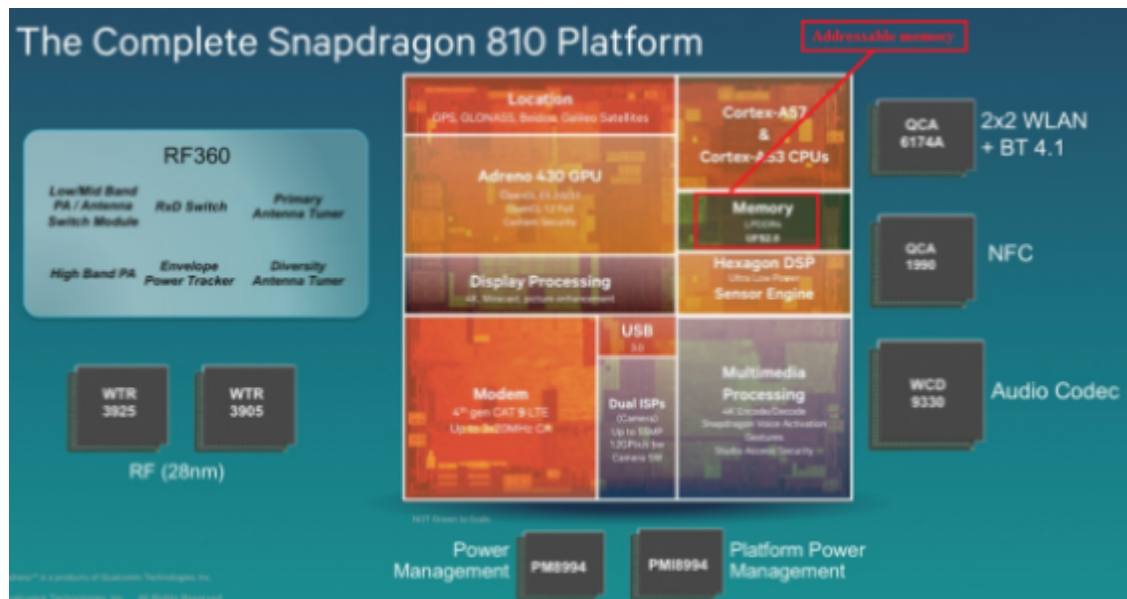
(E.g., <https://www.qualcomm.com/products/snapdragon/processors/810>).

35. The Accused Instrumentality comprises a plurality of media processors (e.g., ARM cortex-A53 multicore processors), each processor receiving at the media processor input/output an instruction and data from the memory, and processing the data responsive to the instruction received to produce at least one result. As previously shown, each ARM cortex-A53 multicore media processor comprises a NEON media coprocessor

which receives instructions and data from memory and processes the data responsive to the instruction received in order to produce a result.



(E.g., <http://www.add.ece.ufl.edu/4924/docs/arm/ARM%20NEON%20Development.pdf>).



(E.g., http://media.bestofmicro.com/L/M/479002/original/Snapdragon_810-Overview.jpg).

L2 memory system

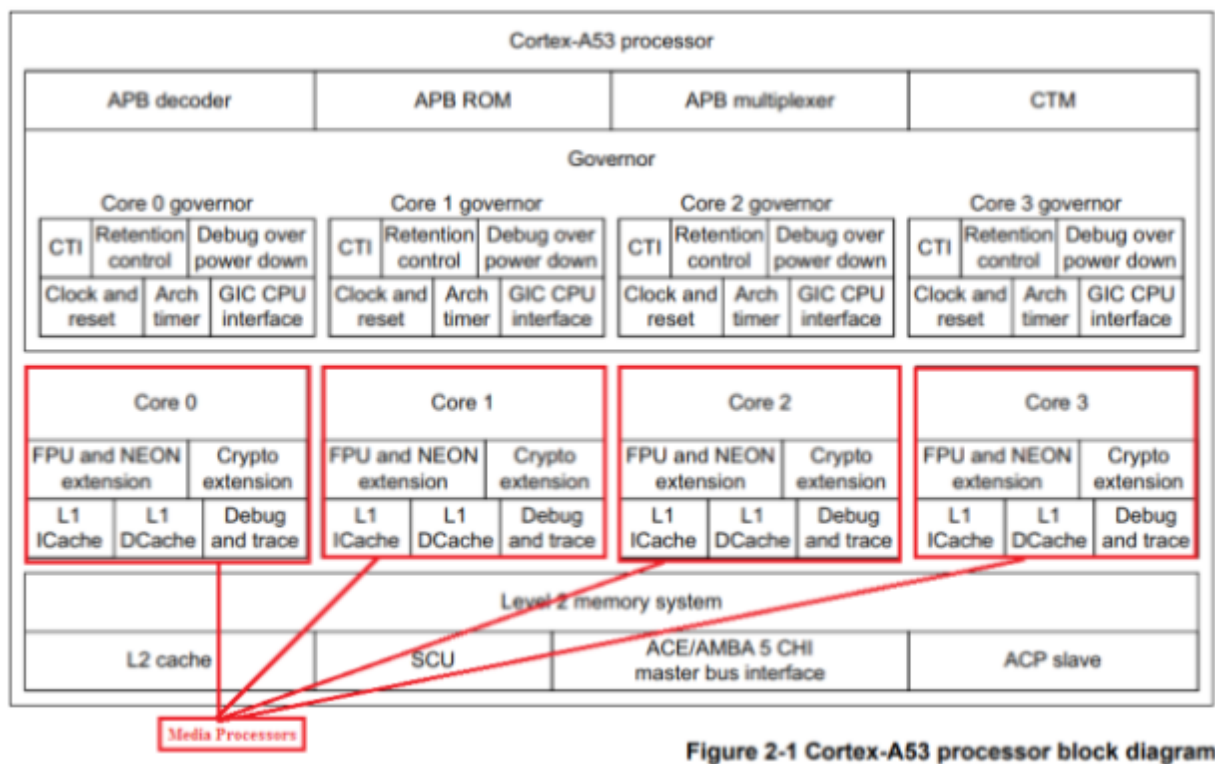
The Cortex-A53 L2 memory system contains the L2 cache pipeline and all logic required to maintain memory coherence between the cores of the cluster. It has the following features:

- An SCU that connects the cores to the external memory system through the master memory interface. The SCU maintains data cache coherency between the cores and arbitrates L2 requests from the cores.

When the Cortex-A53 processor is implemented with a single core, it still includes the Snoop Control Unit (SCU). See *Implementation options* on page 1-7 for more information.

(E.g., [http://docs-api-](http://docs-api-peg.northeurope.cloudapp.azure.com/assets/ddi0500/g/DDI0500G_cortex_a53_trm.pdf)

[peg.northeurope.cloudapp.azure.com/assets/ddi0500/g/DDI0500G_cortex_a53_trm.pdf](http://docs-api-peg.northeurope.cloudapp.azure.com/assets/ddi0500/g/DDI0500G_cortex_a53_trm.pdf)).



(E.g., [http://docs-api-](http://docs-api-peg.northeurope.cloudapp.azure.com/assets/ddi0500/g/DDI0500G_cortex_a53_trm.pdf)

[peg.northeurope.cloudapp.azure.com/assets/ddi0500/g/DDI0500G_cortex_a53_trm.pdf](http://docs-api-peg.northeurope.cloudapp.azure.com/assets/ddi0500/g/DDI0500G_cortex_a53_trm.pdf)).

36. The Accused Instrumentality comprises a plurality of media processors (e.g., ARM cortex-A53 multicore processors), each processor providing at least one of the at least one result at the media processor input/output. (*Supra* ¶34).



HTC ONE M9 32GB Unlocked GSM 20MP Camera Smartphone, Gunmetal Grey

by HTC

★★★★☆ 698 customer reviews | 961 answered questions

Price: **\$196.53**

Color: **Gunmetal Grey**

	\$229.99		\$229.99		\$225.00
	used from \$118.00		\$196.53		

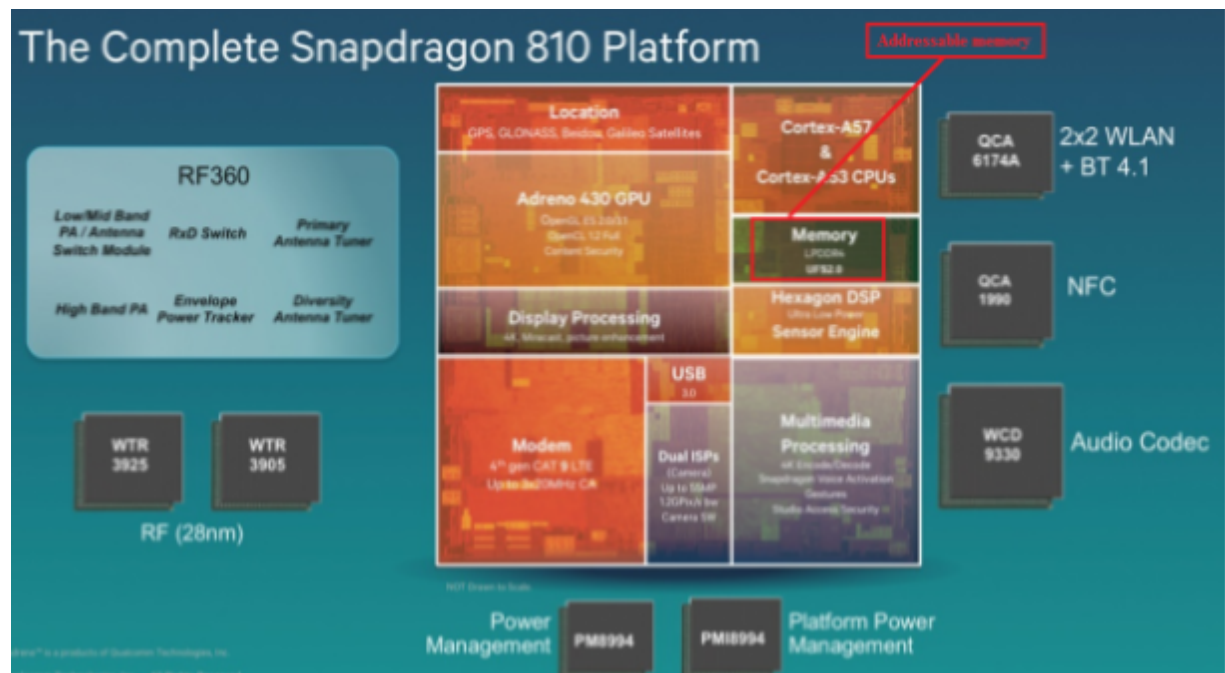
- 20 MP camera with sapphire camera cover lens to deliver crisp clear photos
- Front-facing stereo speakers with built-in amp and Dolby Audio surround for the ultimate audio experience
- The built-in HTC Themes app
- can change the look and feel of your phone
- All-metal body features mirrored edges that are ergonomically tapered to effortlessly fit your grip
- 20 MP camera with sapphire camera cover lens to deliver crisp

(E.g., <https://www.amazon.com/HTC-M9-Unlocked-Smartphone-Gunmetal/dp/B00V4LPCQG>).

The internals remain potent: an octa-core Qualcomm 810 chipset, 3GB of RAM, 2840 mAh battery on top of a Super LCD3 screen. The latter component hasn't got the cachet of Samsung's Super AMOLED display, but it's still color rich and seems close to the glass, which is important for image quality.



(E.g., <https://www.techradar.com/reviews/phones/mobile-phones/htc-one-m9-1285623/review>).



(E.g., http://media.bestofmicro.com/L/M/479002/original/Snapdragon_810-Overview.jpg).

Overview	Documentation
Architecture	Armv8-A
Multicore	1-4x Symmetrical Multiprocessing (SMP) within a single processor cluster, and multiple coherent SMP processor clusters through AMBA 4 technology
ISA Support	<ul style="list-style-type: none"> AArch32 for full backward compatibility with Armv7 AArch64 for 64-bit support and new architectural features TrustZone security technology NEON advanced SIMD DSP & SIMD extensions VFPv4 floating point Hardware virtualization support
Debug & Trace	CoreSight DK-A53

(E.g., <https://developer.arm.com/products/processors/cortex-a/cortex-a53>).

JURY DEMAND

Plaintiff, under Rule 38 of the Federal Rules of Civil Procedure, requests a trial by jury of any issues so triable by right.

November 21, 2018

By /s/Philip P. Mann
Philip P. Mann, WSBA No: 28860
MANN LAW GROUP
107 Spring St.
Seattle, Washington 98104
(206) 436-0900
Fax (866) 341-5140
phil@mannlawgroup.com

David R. Bennett
(Application for Admission *Pro Hac Vice* to be filed)
Direction IP Law
P.O. Box 14184
Chicago, IL 60614-0184
(312) 291-1667
dbennett@directionip.com

Attorneys for Plaintiff Altair Logix
LLC